IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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AMENDMENT

APPLICANT(S): Osawa et al. DOCKET NO.: P97,2636

SERIAL NO: 09/009,248 GROUP ART UNIT: 2814

FILED: January 20, 1998 EXAMINER: D. Graybill

INVENTION: "Lead Frame and Semiconductor Device Having the Same"

Box Non-Fee Amendment
Assistant Commissioner for Patents
Washington, D.C. 20231

S I R:

Applicants submit this Amendment in response to the Office Action mailed October 28, 1999. Applicants request amendment, reconsideration, and allowance of the patent application.

IN THE CLAIMS:

Please amend claims 1, 3, and 5 as follows:

1. (Amended) A semiconductor device comprising:

a semiconductor chip having a plurality of electrode pads formed at a periphery of a front surface thereof;

a wiring film formed on a front surface side of said semiconductor chip by laminating an insulation film on a lead pattern;

an outer connection terminal formed so as to protrude above said wiring film;

a plurality of leads extending from said wiring film and connected to the electrode pads on said semiconductor chip at extended tip ends thereof;

an external ring provided so as to surround said semiconductor chip and formed with a plurality of through holes or blind holes positioned entirely outside of a perimeter edge of the semiconductor chip; and

a sealing resin filled between said semiconductor chip and said external ring.

3. (Amended) A lead frame comprising:

a wiring film formed by laminating an insulation film on a lead pattern;

an external connection terminal formed so as to protrude above said wiring film;

a plurality of leads extending from said wiring film and forming connecting portions to electrode pads on a semiconductor chip at extended tip ends thereof; and

an external ring provided outside said wiring film, having an opening portion capable of housing said semiconductor chip and formed with a plurality of through holes or blind holes positioned entirely outside of a perimeter edge of the semiconductor chip when the opening portion houses the semiconductor chip.

5. (Amended) An electronic apparatus including a printed wiring board loaded with a semiconductor chip, said semiconductor device comprising:

a semiconductor chip having a plurality of electrode pads formed at a periphery of a front surface thereof;

a wiring film formed on a front surface side of said semiconductor chip by laminating an insulation film on lead patterns;

an outer connection terminal formed so as to protrude above said wiring film;

a plurality of leads extending from said wiring film and connected to the electrode pads on said semiconductor chip at extended tip ends thereof;

an external ring provided so as to surround said semiconductor chip and, formed with a plurality of through holes or blind holes positioned entirely outside of a perimeter edge of the semiconductor chip; and

a sealing resin filled between said semiconductor chip and said external ring, wherein said external connection terminal and an electrode on said printed wiring board are connected.

Please add claims 10-12 as follows:

10. A semiconductor device according to claim 1, wherein the external ring has an open top and an open bottom and is entirely spaced away from the semiconductor chip.

11. A lead frame device according to claim 3, wherein the external ring has an open top and an open bottom and is entirely spaced away from the semiconductor chip when the opening portion houses the semiconductor chip.

12. An electronic apparatus according to claim 5, wherein the external ring has an open top and an open bottom and is entirely spaced away from the semiconductor chip.

REMARKS

The Office Action was issued on pending claims 1-9, in which claims 1-6 were rejected and claims 7-9 were withdrawn from consideration. Claims 1, 3, and 5 have been amended, no claims have been canceled, and claims 10-12 have been added. Thus, claims 1-12 are pending in the case, with claims 1-6 and 10-12 under consideration and claims 7-9 being withdrawn from consideration.

In the Office Action, claims 1-6 were rejected under 35 U.S.C. §103(a) as being unpatentable over the combination of Takahashi et al., U.S. Patent No. 5,198,883 and Park et al., U.S. Patent No. 5,847,446. Applicants respectfully disagree.

Applicants' invention, as claimed in claim 1, pertains to a semiconductor device. Claim 1 calls for a semiconductor chip having a plurality of electrode pads formed at a periphery of a front surface thereof, a wiring film formed on a front surface side of said semiconductor chip by laminating an insulating film on a lead pattern, and an outer connection terminal formed so as to protrude above said wiring film. Claim 1 further calls for a plurality of leads extending from said wiring film and connected to the electrode pads on said semiconductor chip at extended chip ends thereof. Claim 1 also calls for an external ring provided so as to surround said semiconductor chip and formed with a plurality of through holes or blind holes positioned entirely outside of a perimeter edge of the semiconductor chip. Claim 1 further calls for a sealing resin filled between said semiconductor chip and said external ring.

One example of Applicants' claimed semiconductor device is shown in Fig. 4. The semiconductor device 1 has a semiconductor chip 2 having a plurality of electrode pads 3 formed at a periphery of a front surface of the semiconductor chip 2. A wiring film 5 is formed on a front surface side of the semiconductor chip 2 by laminating an insulation film 7 on a lead pattern 6. An outer connection terminal 8 is formed so as to protrude above the wiring film 7. A plurality of leads 9 extend from the wiring film 5 and are connected to the electrode pads 3 on the semiconductor chip 2 at extended tip ends thereof. An external ring 11 is provided so as to surround the semiconductor chip 2 and is formed with a plurality of through holes 15 or blind holes 16 (Fig. 7). Referring to Figs. 4 and 5, the plurality of through holes 15 or blind holes 16 are positioned entirely outside of a perimeter edge of the semiconductor chip 2. A sealing resin 12 is filled between the semiconductor chip 2 and the external ring 11.

Applicants' claimed semiconductor device is an improvement over existing semiconductor devices. For example, because Applicants' semiconductor device has a sealing ring having a plurality of through holes or blind holes, the sealing resin is filled in the plurality of through holes or blind holes and increases the area of contact between the sealing resin and the external ring. The bonding strength

of the sealing ring is improved and the sealing resin is more rigidly secured to the external ring. See the specification at page 20, lines 16-22.

As mentioned above, the semiconductor device, as claimed in claim 1, calls for an external ring provided so as to surround said semiconductor chip and formed with a plurality of through holes or blind holes. Claim 1 has been amended to further define the position of the plurality of through holes or blind holes. Specifically, claim 1 now calls for the plurality of through holes or blind holes to be positioned entirely outside of a perimeter edge of the semiconductor chip. This amendment to claim 1 is supported by Figs. 4 and 5 which show the through holes 15 as being positioned entirely outside of a perimeter edge of the semiconductor chip 2.

Park et al. pertains to a semiconductor package having a chip attach pad with perimeter slots. Referring to Figs. 3-5 of Park et al., Park et al. shows a semiconductor chip package 200 having a semiconductor chip 110 bonded on a chip attach pad 120. The chip attach pad 120 has slots 124 formed in a perimeter region of the chip attach pad 120. The slots 124 in the chip attach pad 120 are formed in the perimeter region corresponding to edges 110a, 110b of the semiconductor chip 110. In other words, the edges 110a, 110b of the chip 110 are located along the slots 124. This structure of the slots 124 being positioned at the edges of the semiconductor chip 110 in Park et al. is provided so that molding compound 160 within the slots 124 directly adheres to the lower surfaces 111a, 111b of the semiconductor chip edges 110a, 110b. See Park et al., column 3, lines 56-67. Because Park et al. provides the slots 124 in the chip attach pad 120 at the edges of the semiconductor chip 110 so that the molding compound 160 can adhere to the semiconductor chip 110, Applicants respectfully submit that there is no suggestion, motivation, or incentive to move the slots 124 entirely outside of the perimeter edges of the semiconductor chip 110. Such a modification to the slots 124 in Park et al. would not achieve the objective of providing molding compound 160 to adhere to the underside edge of the semiconductor chip 110.

Takahashi et al. pertains to a semiconductor device having an improved lead arrangement and method of manufacturing the same. The Office Action acknowledges that Takahashi et al. does not appear to explicitly teach an external ring formed with a plurality of through holes. Accordingly, Applicants respectfully submit that the combination of Takahashi et al. with Park et al. does not result in Applicants' claimed invention. In particular, if Takahashi et al. is modified to include the slots 124 of Park et al., the Takahashi et al. semiconductor device would have slots positioned at the peripheral edge of the semiconductor chip rather than being positioned entirely outside of the perimeter edge of the semiconductor chip.

Applicants' invention, as claimed in claims 3 and 5, also call for the plurality of through holes or blind holes to be positioned entirely outside of a perimeter edge of the semiconductor chip.

Thus, Applicants respectfully submit that the §103(a) rejection of claims 1-6 has been overcome.

CONCLUSION

For the foregoing reasons, Applicants submit that the patent application is in condition for allowance and request a notice of allowance to that effect.

Respectfully submitted,

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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Box Non-Fee Amendment, Assistant Commissioner for Patents, Washington, D.C. 20231 on January 28, 2000.